

# 2SJ549(L),2SJ549(S)

Silicon P Channel MOS FET  
High Speed Power Switching

# HITACHI

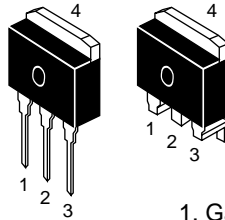
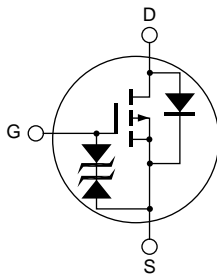
ADE-208-644A (Z)  
2nd. Edition  
Jun 1998

## Features

- Low on-resistance  
 $R_{DS(on)} = 0.11 \Omega$  typ.
- Low drive current
- 4 V gate drive devices
- High speed switching

## Outline

LDPAK



1. Gate
2. Drain
3. Source
4. Drain

## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	-60	V
Gate to source voltage	$V_{GSS}$	±20	V
Drain current	$I_D$	-12	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	-48	A
Body-drain diode reverse drain current	$I_{DR}$	-12	A
Avalanche current	$I_{AP}$ <sup>Note3</sup>	-12	A
Avalanche energy	$E_{AR}$ <sup>Note3</sup>	12	mJ
Channel dissipation	$P_{ch}$ <sup>Note2</sup>	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

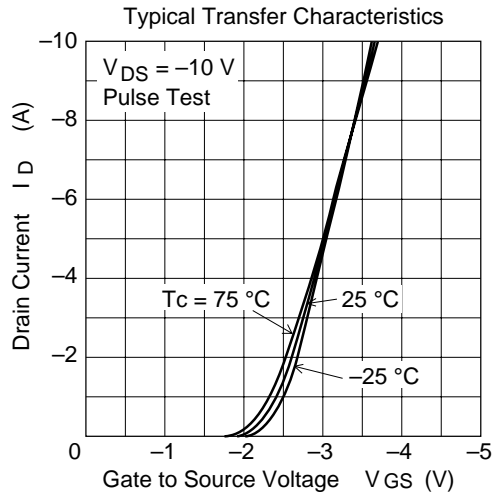
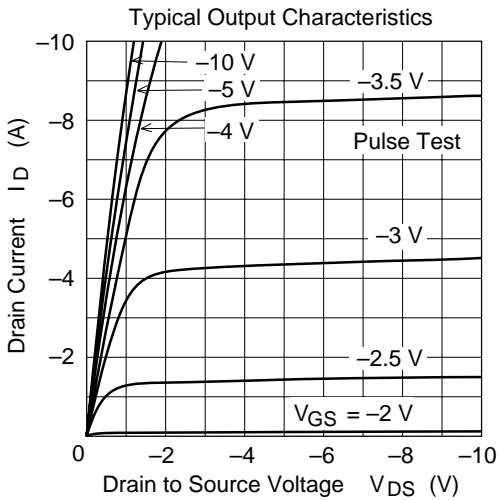
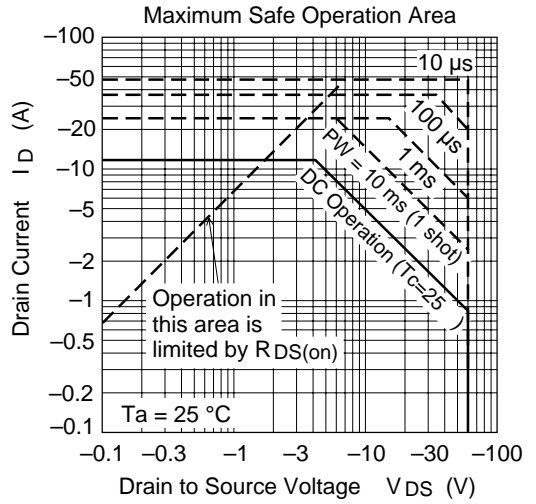
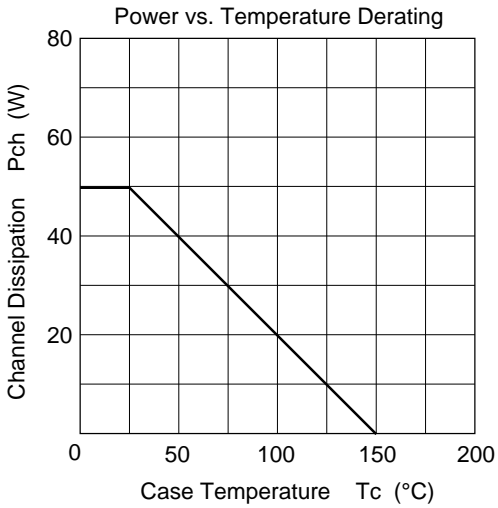
Note: 1.  $PW \leq 10\mu s$ , duty cycle  $\leq 1\%$   
 2. Value at  $T_c = 25^\circ C$   
 3. Value at  $T_{ch} = 25^\circ C$ ,  $R_g \geq 50\ \Omega$

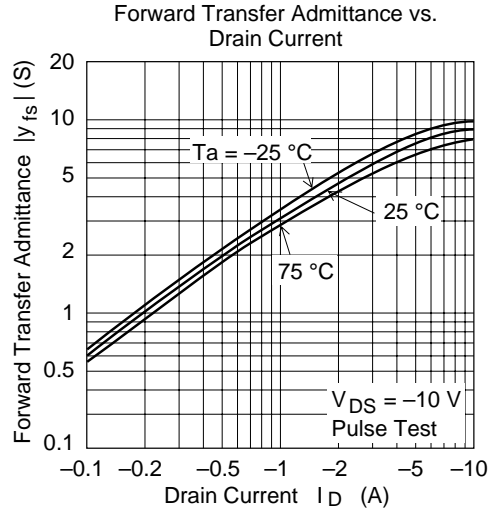
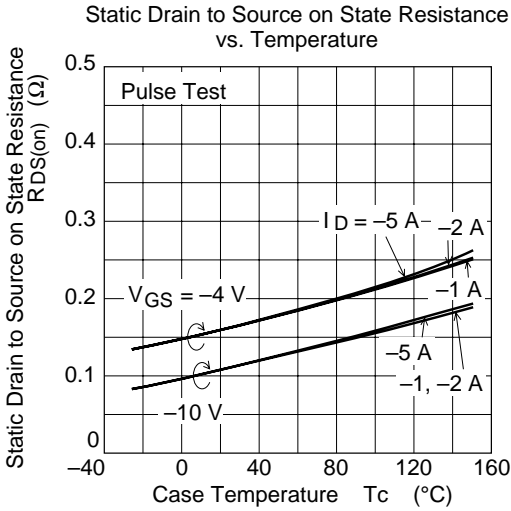
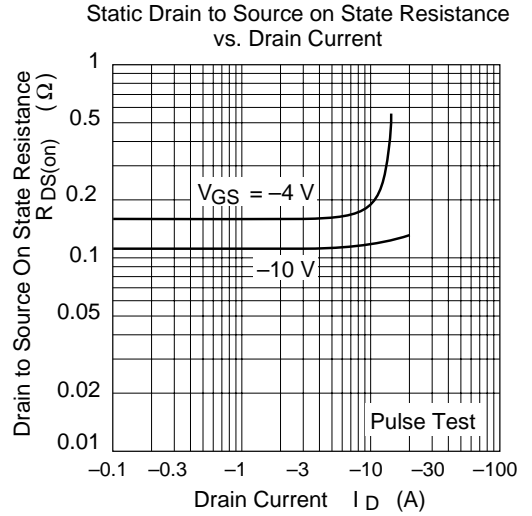
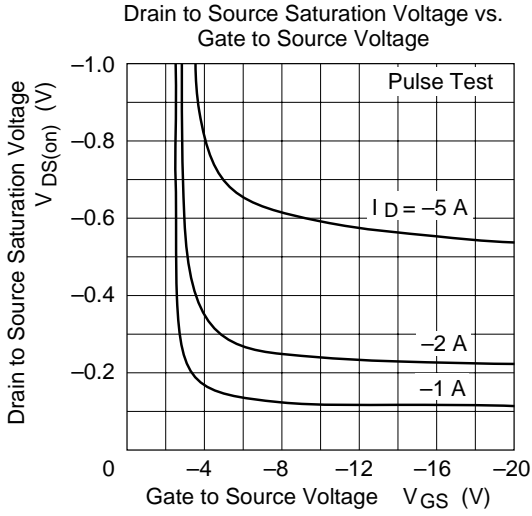
## Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10mA$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100\mu A$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-10	μA	$V_{DS} = -60V$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±10	μA	$V_{GS} = \pm 16V$ , $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -1mA$ , $V_{DS} = -10V$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.11	0.15	Ω	$I_D = -6A$ , $V_{GS} = -10V$ <sup>Note4</sup>
	$R_{DS(on)}$	—	0.16	0.23	Ω	$I_D = -6A$ , $V_{GS} = -4V$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	5	8	—	S	$I_D = -6A$ , $V_{DS} = -10V$ <sup>Note4</sup>
Input capacitance	Ciss	—	580	—	pF	$V_{DS} = -10V$
Output capacitance	Coss	—	300	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	85	—	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	$V_{GS} = -10V$ , $I_D = -6A$
Rise time	$t_r$	—	55	—	ns	$R_L = 6\Omega$
Turn-off delay time	$t_{d(off)}$	—	85	—	ns	
Fall time	$t_f$	—	60	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	-1.2	—	V	$I_D = -12A$ , $V_{GS} = 0$
Body-drain diode reverse recovery time	$t_{rr}$	—	60	—	ns	$I_F = -12A$ , $V_{GS} = 0$ $di_F/dt = 50A/\mu s$

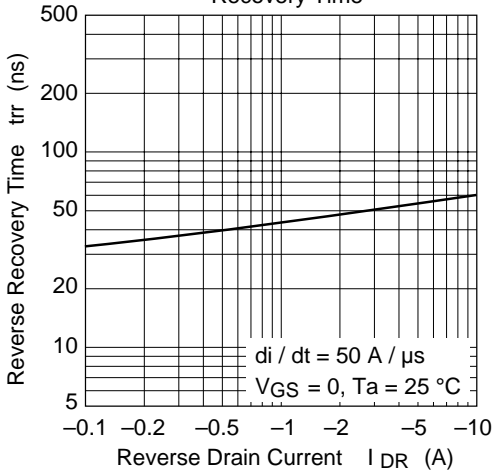
Note: 4. Pulse test

Main Characteristics

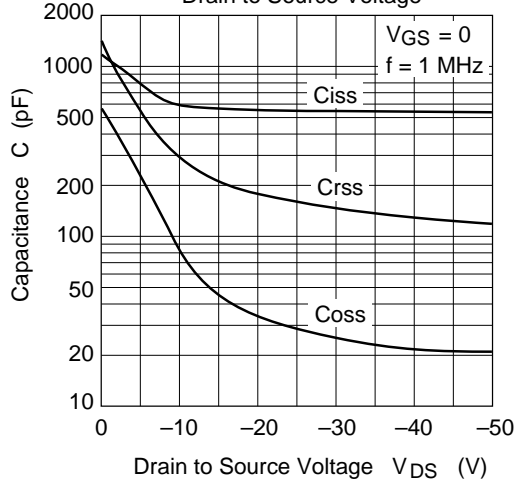




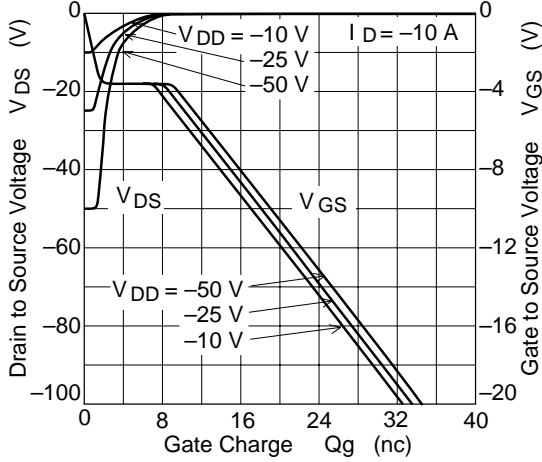
Body-Drain Diode Reverse Recovery Time



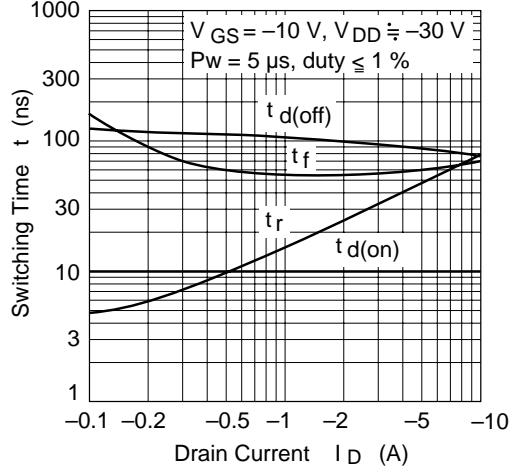
Typical Capacitance vs. Drain to Source Voltage

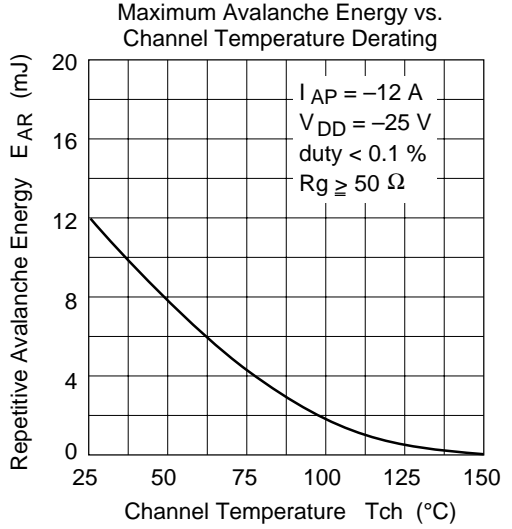
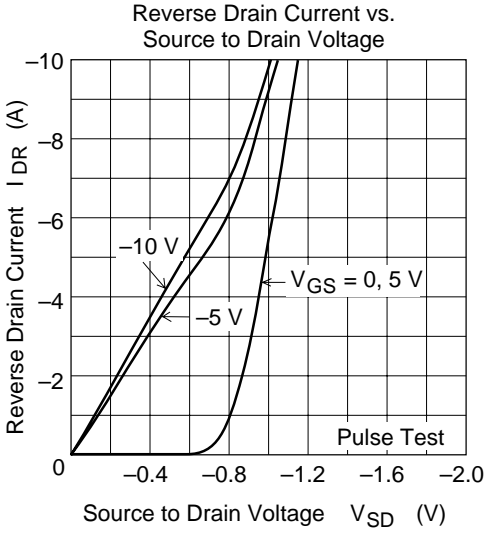


Dynamic Input Characteristics

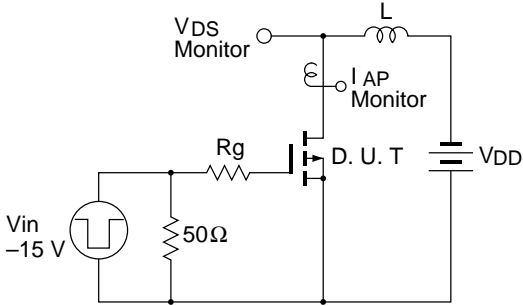


Switching Characteristics



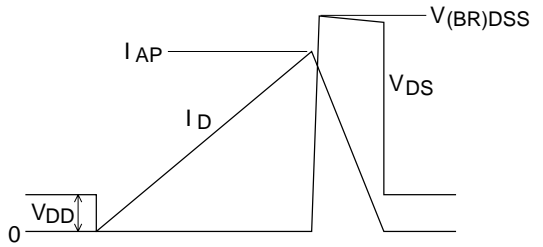


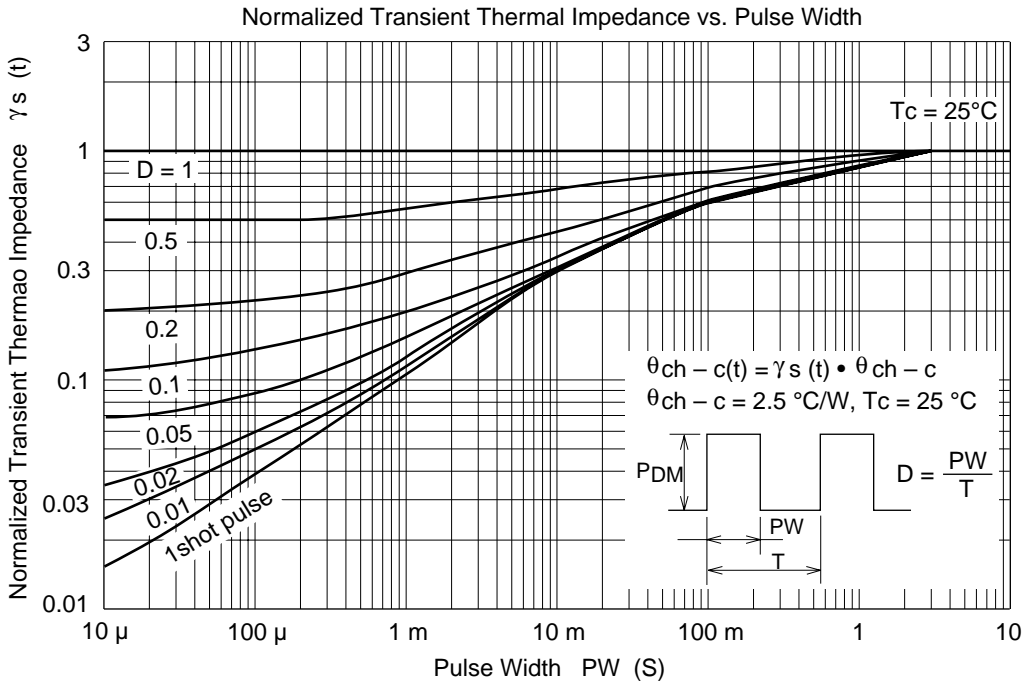
Avalanche Test Circuit



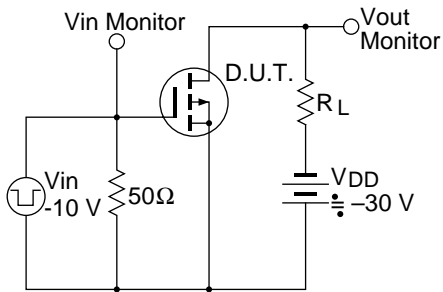
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

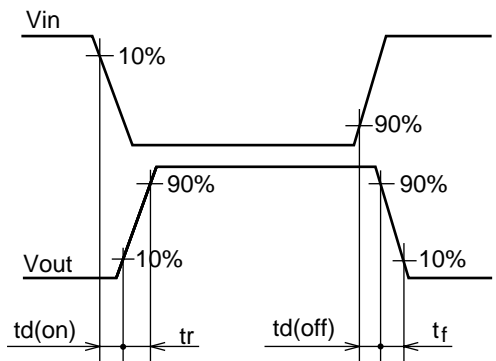




Switching Time Test Circuit

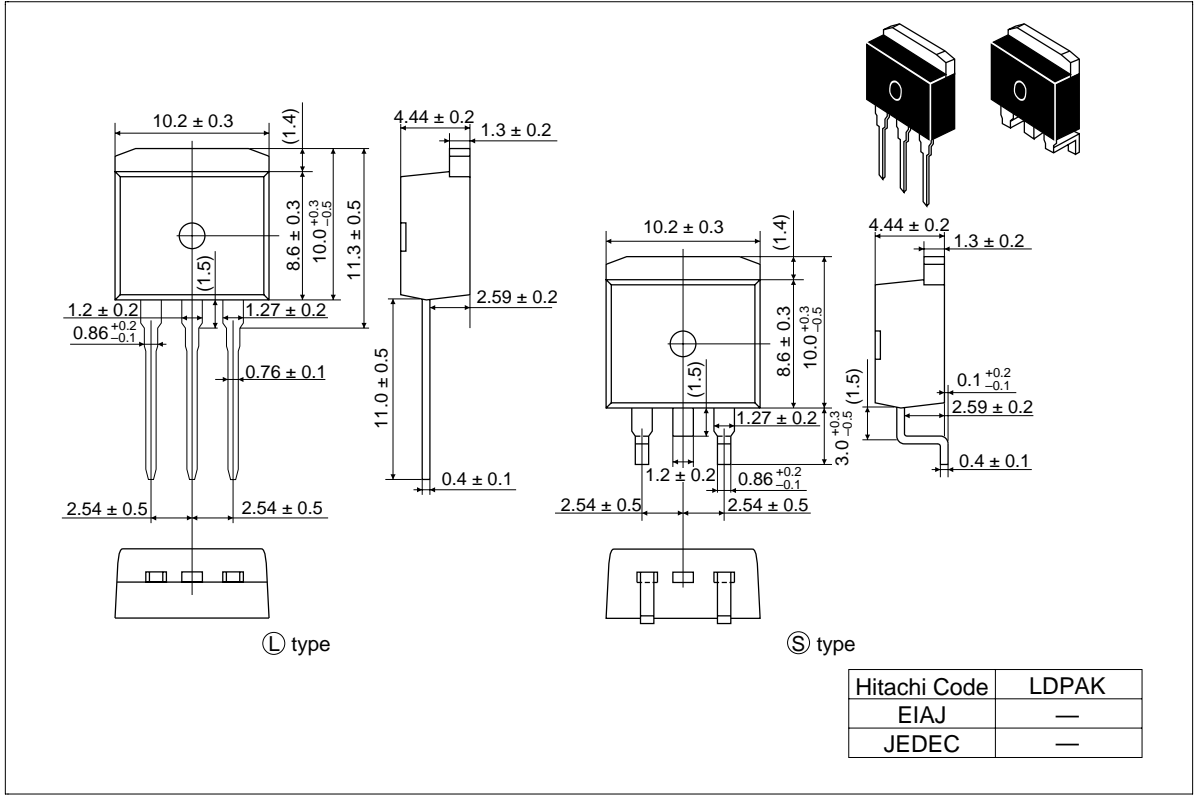


Waveform



Package Dimensions

Unit: mm





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